1. An instruction decoding unit in a microcomputer comprising:

an instruction register storing instructions fetched from a memory;

an instruction decoder decoding instruction codes of the instructions stored in the instruction register and for designating micro-instructions to be executed based on the decoded instruction codes;

a micro-ROM outputting the micro-instructions designated by the instruction decoder; and

a user instruction selector selecting or changing the micro-instructions from the micro-ROM in response to a selection by a user so as to change an operation of an instruction word corresponding to the instruction being fetched without any subsequent intervening storage of the micro-instructions in RAM.

2. The instruction decoding unit in a microcomputer as claimed in claim 1, wherein the user instruction selector selects the micro-instructions using a mask option or a particular register.

3. An instruction decoding unit in a microcomputer comprising:

an instruction register storing instructions fetched from a memory;

an instruction decoder decoding instruction codes of the instructions stored in the instruction register and designating micro-instructions to be executed;

an instruction code selector, connected between the instruction register and the instruction decoder, allowing a user to select a signal corresponding to at least one of a

plurality of instruction maps wherein said instruction code selector is operable to encrypt instruction code;

a micro-ROM outputting a series of the micro-instructions designated by the instruction decoder.

4. The instruction decoding unit in a microcomputer as claimed in claim 3, further comprising:

a user instruction selector selecting or changing the micro-instructions of the micro-ROM in response to a selection by a user so as to change the operation of an instruction word.

5. The instruction decoding unit in a microcomputer as claimed in claim 4, wherein the user instruction selector selects the instructions using a mask option or a particular register.

6. The instruction decoding unit in a microcomputer as claimed in claim 3, wherein the plurality of instruction maps are two or more.

7. An instruction decoding unit in a microcomputer, comprising:

an instruction code selector generating encrypted instructions by manipulating received instructions; and

a decoder decoding instructions corresponding to encrypted instructions received from the instruction code selector.

8. The instruction decoding unit recited by claim 7, further comprising:

a user instruction selector selecting or changing the instructions decoded by the decoder in response to a selection by a user.

9. An apparatus to provide microcodes comprising:

a ROM storing a plurality of microcodes;

an instruction processor receiving instructions from a user and instructing the ROM to output a first microcode; and

a selector allowing the user to selectively modify the microcodes stored in the ROM, to output a second microcode without any subsequent intervening storage of the microcodes in RAM,

the first and second microcodes being combined to form a control signal.

10. The apparatus of claim 9, wherein the selector outputs the second microcode by increasing, decreasing or inverting the microcodes stored in the ROM.

11. The apparatus of claim 9, wherein the selector comprises a switch operated by map selecting bits determined according to a number of instruction maps.

12. The apparatus of claim 9, wherein the instruction processor further comprises:

an instruction register storing instructions fetched from a memory; and

an instruction decoder decoding instruction codes of the instructions stored in the instruction register and designating micro-instructions to be executed based on the decoded instruction codes.

13. The apparatus of claim 12, wherein the instruction processor further comprises an instruction code selector, connected between the instruction register and the instruction

decoder, allowing a user to select a signal pertaining to a plurality of instruction maps.

14. The apparatus of claim 13, wherein the instruction code selector rearranges a plurality of bits received from the instruction register based on the instruction maps, and applies a plurality of map selecting bits to the rearranged bits to allow subsequent reconstruction by the instruction decoder.

15. The instruction code selector of claim 3, wherein said instruction code selector is operable to receive a data instruction from the instruction register, and append map selecting bits to the data instruction, wherein said map selecting bits correspond to an instruction map selected by a user, thereby performing encryption of the instruction code.